N.R. Ilnytskyi[1], T.R. Sorokhtey[2], V.M. Umantsiv[2], L.I. Nykyruy[2], M.F. Pavlyuk[2], R.V. Ilnytskyi[2]

Design of digital-to-analogue signal converters for sensor microsystems on a crystal

[1]Ivano-Frankivsk National Medical University, Ivano-Frankivsk, Ukraine;
[2]Vasyl Stefanyk Precarpathian National University, Ivano-Frankivsk, Ukraine, roman.ilnitsky@pnu.edu.ua

The results of computer simulation of the developed R-2R digital-to-analogue converter design are given. Results with output voltage values for different digital input code are also given. The topology of such device is proposed, and its operation is modulated. Thus, the MicroWind software application was used to modelling and develop the operation of the digital signal to analogue converter, as it is an open-source software tool for all users, which allows the design and simulation of an integrated circuit at the physical description (IC) level.

Keywords: digital-to-analogue converter, MicroWind software, submicron technology.

Introduction

The software application MicroWind 3.1 was used to model and develop the operation of the digital signal to analog converter, as it is an open source software tool for all users, which allows the design and simulation of an integrated circuit at the physical description (IC) level. Also, the DSCH3.5 program is a logic editor and simulator of electronic circuits. DSCH3.5 is used to verify the architecture of the logic circuit before starting the microelectronics design. DSCH provides a user-friendly hierarchical logic design and simulation environment with delay analysis that enables the design and verification of complex logic structures. Therefore, these tools were used to simulate DAC operation.

I. Results and discussion

For modeling and topology development, the R-2R DAC, which is quite simple in its design, is well suited. According to the scheme of this converter, its model was designed in the DSCH software application.

Accordingly, this model consists of three resistors with a nominal value of 1 kΩ and five resistors with a nominal value of 2 kΩ (although twice smaller parameters were used in the future), in addition to them, there are four n-type KMON transistors in the circuit, to which digital signals are fed. In our case, the digital zero is 0V, and the unit is 1.2V. In the circuit in DSCH, this can be implemented using a simple electrical switch. In order to transfer the converter circuit from DSCH to the environment with the physical modeling layer of MicroWind, it is necessary to design the topology for this device. Figures 2 and 3 show the KMON resistor and transistor models used in the simulation. Resistors have a typical appearance for KMON technology and are made of polysilicon. The 2R resistors were modeled manually, not using the layout generator automation tool. The transistors also have a fairly typical topology, the gates are fed a digital signal, the drain is grounded, and the drain is connected to the R-2R resistor matrix.

The resolution of the R-2R DAC is related to the accuracy of the resistors and the resistance of the switches, which must be small to avoid voltage drops and some non-linearity. It is important to implement a switch with low on-resistance (large width, minimum length) along with large resistors R. To compensate for the on-resistance of the nMOS

device, a dummy switch whose on-resistance is half the on-resistance can be inserted in each cell in series with R.

Fig. 4 shows the construction of a four-bit digital-to-analog signal converter at the physical level, developed using MicroWind 3.1. As mentioned earlier, the resistors have ratings twice as small as in the DSCH model – 500 Ohms and 1 kOhms.

In fig. 5 shows a three-dimensional image of the digital-to-analog converter. Numbers indicate the main details of the scheme: 1 – zones to which the digital code is applied; 2 – KMON transistors; 3 – VSS-, grounding; 4 – KMON resistors;

5 – VDD+, 1.2V power source. Fig. 5 shows the result of the circuit simulation with the digital code 0100, the value differs from that given in Table 1.

Due to the growing popularity of monolithic systems on a crystal, i.e., MEMS, the DAC must be implemented in low-voltage submicron CMON technology to achieve low manufacturing costs and to be able to integrate with other circuits. Therefore, the topology of such a device was developed and its operation was modulated. In addition, this version of the DAC can be improved in the effective use of the area of the silicon crystal.
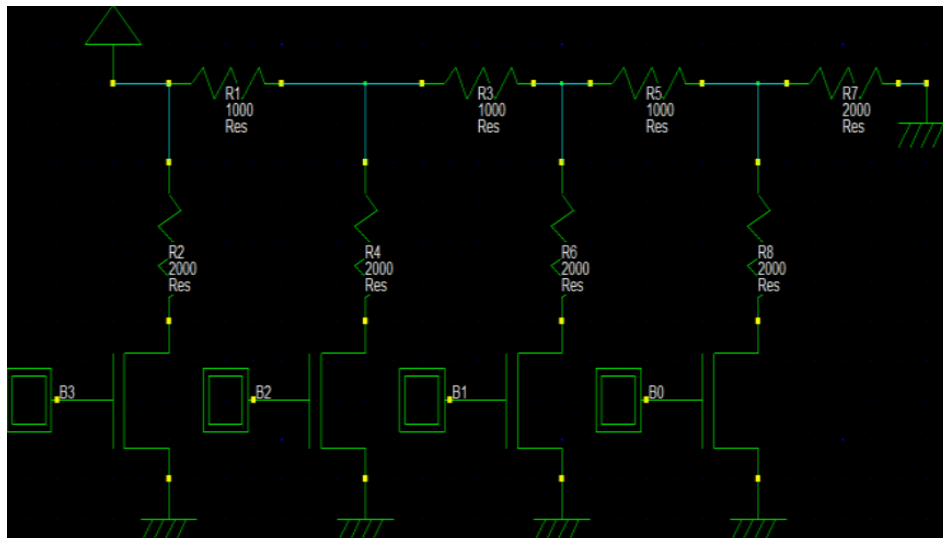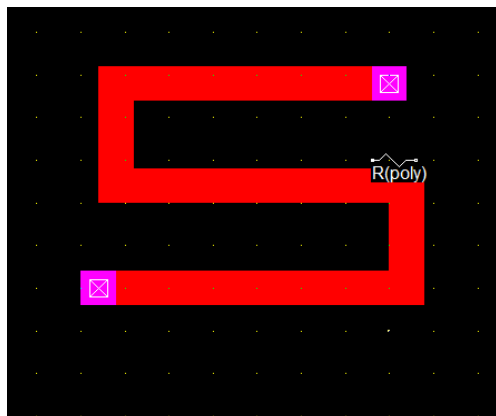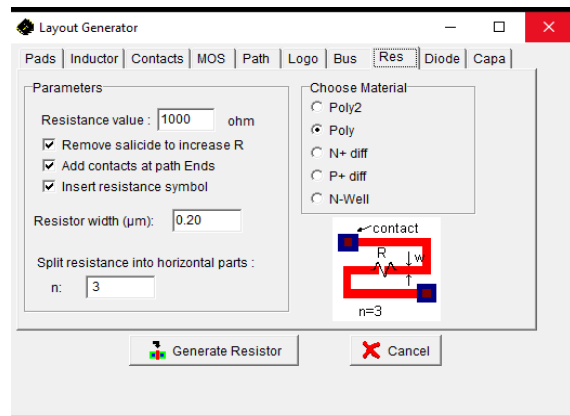

Fig. 1. Model R-2R DAC in DSCH 3.5.
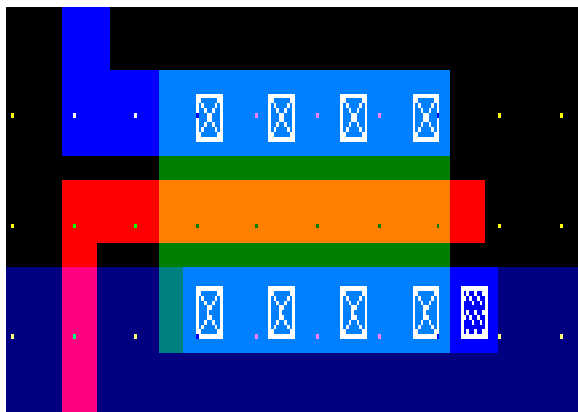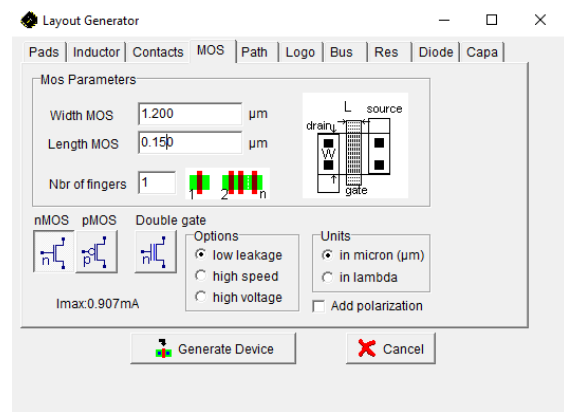

a)   b)

Fig. 2. KMON resistor a) and its generation process b) in MicroWind 3.1

a)   b)

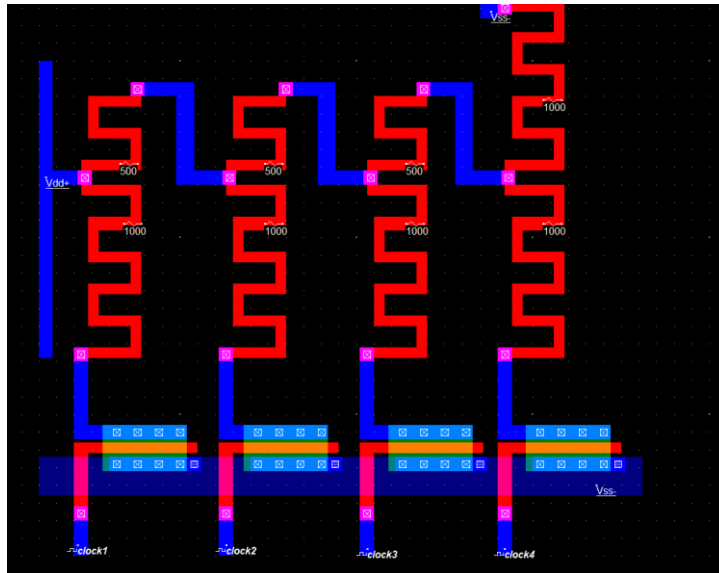**Fig. 3.** KMON transistor a) and its generation process b) in MicroWind 3.1.
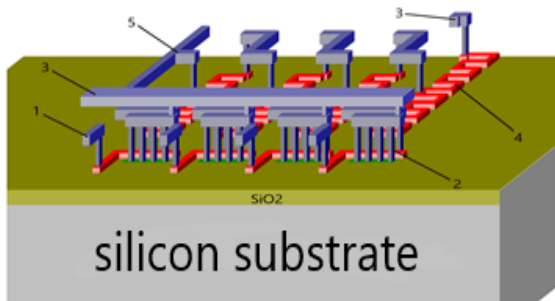
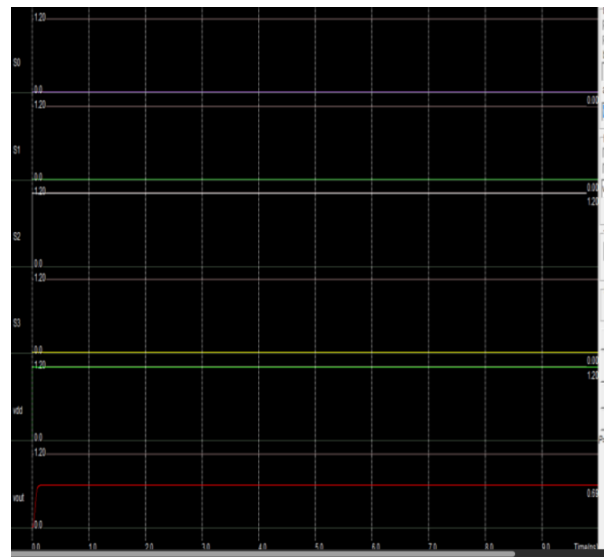**Fig. 4.** Topology of R-2R DAC in MicroWind 3.1.

Fig. 5. 3D image R-2R DAC.

Fig. 6. Simulation results for the digital code 0100.

Table 1

Simulation results of the R-2R DAC.

Decimal code	Digital code				Output voltage	
	B1	B2	B3	B4	Theoretical	Real
0	0	0	0	0	1.2	1.2
1	0	0	0	1	1.125	1.15
2	0	0	1	0	1.05	0.93
3	0	0	1	1	0.975	0.87
4	0	1	0	0	0.9	0.69
5	0	1	0	1	0.825	0.64
6	0	1	1	0	0.75	0.53
7	0	1	1	1	0.675	0.5
8	1	0	0	0	0.6	0.35
9	1	0	0	1	0.525	0.29
10	1	0	1	0	0.45	0.24
11	1	0	1	1	0.375	0.22
12	1	1	0	0	0.3	0.15
13	1	1	0	1	0.225	0.11
14	1	1	1	0	0.15	0.09
15	1	1	1	1	0.075	0.07

The results of the simulation of the operation of the scheme in the MicroWind software are shown in Table 1. The discrepancy in the obtained results is not a critical problem since there are no coincidences in the simulation results with different digital codes. This allows you to build a truth table based on actual results.

Conclusion

The architecture of developed DACs is simple, with an output voltage (but the output impedance depends on the digital code) that is inherently monotonic, even if a resistor is accidentally short-circuited, output n cannot exceed output (n + 1). It is linear if all resistors are equal but can be made intentionally non-linear if a non-linear DAC is required. Because only two switches are active during a transition, this is a low-failure architecture present. Additionally, the switching failure is code-independent, making it ideal for low-distortion applications. Since the glitch is relatively constant regardless of the code transition, the frequency content of the glitch corresponds to the DAC refresh rate and its harmonics, not to the harmonics of the DAC fundamental output frequency. The main disadvantage of a line DAC is the large number of resistors and switches required for high resolution, and as a result it was not commonly used as a simple DAC architecture until the recent advent of very small IC function sizes made it very practical for low to mid-range DACs resolution. Today, this architecture is quite widely used in simple DACs such as digital potentiometers.

Ilnytskyi N.R. – student;
Sorokhtey T.R. – Ph.D.-student;
Umantsiv V.M. – Ph.D., researcher;
Pavlyuk M.F. – Ph.D., Associate Professor of the Department of Computer Engineering and Electronics;
Nykyruy L.I. – Ph.D., Professor, Head of the Department of Physics and Chemistry of Solid State;
Ilnytskyi R.V. – Doctor of Physical and Mathematical Sciences, Professor Department of Materials Science and New Technologies.

[1] S. Balasubramanian, V. J.Patel, & W. Khalil, *Current and Emerging Trends in the Design of Digital-to-Analog Converters*. In: Carbone, P., Kiaei, S., Xu, F. (eds) Design, Modeling and Testing of Data Converters. Signals and Communication Technology. Springer, Berlin, Heidelberg, 83 (2014); https://doi.org/10.1007/978-3-642-39655-7_3.

[2] K. V. Ogorodnyk, B. P. Knysh, P. M. Ratushny, O. O. Lazarev, *Modeling in electronics: a study guide*. VNTU, Vinnytsia, 118 p. (2017).

[3] O. Aiello, P. Crovetti, & M. Alioto. *Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation,* IEEE Transactions on Circuits and Systems, 66(8), 70890 (2020); https://doi.org/10.1109/ACCESS.2020.2986949.

[4] M. Gustavsson, J. J. Wikner, N. N. Tan, M. Gustavsson, J. J. Wikner, & N. N. Tan. *Overview of D/A Converter Architectures*, CMOS Data Converters for Communications, 87 (2002); https://doi.org/10.1007/0-306-47305-4_4.

[5] Jaime Castillo-Leon, Winnie Svendsen, Maria Dimaki, Valentina Arima, Muhammad Akram, Sandrine Miserere, Christiane Neumann, G. Kipling. *Lab-on-a-Chip Devices and Micro-Total Analysis Systems,* A Practical Guide (2015); https://doi.org/10.1007/978-3-319-08687-3.

[6] Athanasios Giannitsis. *Microfabrication of biomedical lab-on-chip devices. A review*, Estonian Journal of Engineering, 17, 109 (2011); https://doi.org/10.3176/eng.2011.2.03.

[7] P. Abgrall and A.-M. Gué. *Lab-on-chip technologies: making a microfluidic network and coupling it into a complete microsystem—a review*, J. Micromech. Microeng., 17 R15 (2007); https://doi.org/10.1088/0960-1317/17/5/R01.

[8] D.C. Duffy, J. Cooper McDonald, O. J. A. Schueller and G. M. Whitesides. *Rapid prototyping of microfluidic systems in poly(dimethylsiloxane)*, Anal. Chem., 70, 4974 (1998); https://doi.org/10.1021/ac980656z.

[9] S. Zare Harofte, et al., *Recent Advances of Utilizing Artificial Intelligence in Lab on a Chip for Diagnosis and Treatment*, Small, 18(42), 2203169 (2022); https://doi.org/10.1002/smll.202203169.

[10] S.-I. Funano, N. Ota, and Y. Tanaka. *A simple and reversible glass–glass bonding method to construct a microfluidic device and its application for cell recovery*, Lab on a Chip, 21(11), 2244 (2021); https://doi.org/10.1039/D1LC00058F.

Н.Р. Ільницький[1], Т.Р. Сорохтей[2], В.М. Уманців[2], М.Ф. Павлюк[2], Л.І. Никируй[2], Р.В. Ільницький[2]

Проектування цифро-аналогових перетворювачів сигналів для сенсорних мікросистем на кристалі

[1]Прикарпатський національний університет імені Василя Стефаника, Івано-Франківськ, Україна,
lyubomyr.nykyruy@pnu.edu.ua
[2]Івано-Франківський національний медичний університет, Івано-Франківськ, Україна

Наведено результати комп'ютерного моделювання розробленої конструкції цифро-аналогового перетворювача P-2P, а також результати зі значеннями вихідної напруги для різних цифрових вхідних кодів. Запропоновано топологію такого пристрою та модульовано його роботу. Таким чином, програмний додаток MicroWind використовувався для моделювання та розробки роботи перетворювача цифрового сигналу в аналоговий, оскільки це програмний інструмент із відкритим кодом для всіх користувачів, який дозволяє проектувати та моделювати інтегральну схему за фізичним описом (ІС) рівень.

Ключові слова: цифро-аналоговий перетворювач, програмне середовище MicroWind, субмікронна технологія.