PHYSICS AND CHEMISTRY OF SOLID STATE
V. 24, No. 4 (2023) pp. 603-609

Section: Technology

DOI: 10.15330/pcss.24.4.603-609

Vasyl Stefanyk Precarpathian National University

ФІЗИКА І ХІМІЯ ТВЕРДОГО ТІЛА
Т. 24, № 4 (2023) С. 603-609

Технічні науки

PACS: 85.60. Dw.

ISSN 1729-4428

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The influence of the structure of guard rings on the dark currents of silicon *p-i-n* photodiodes

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The article examines the influence of the guard rings (GR) system structure on the dark currents of responsive elements (RE) and the actual guard rings of silicon 4-element *p-i-n* photodiodes (PD). The samples were made on the basis of *p*-silicon by planar technology. Samples with one, two, and three GR were produced. It was found that increasing the amount of n^+-GRs does not reduce the dark current of the REs. But with an increase in the number of n^+-GRs, the probability of an edge breakdown of the n^+-*p*-junction in the regions of the exit of the hetero-junction of the GR to the surface increases. It is possible to reduce the levels of dark current of REs and GR by combining n^+- and p^+- guard regions, where p^+-GR is a region of restriction of dark current leakage channels, isotypic with the substrate material. PD was made with p^+-GR on the periphery of the crystal in the form of a concentric ring, as well as with a p^+- region on the entire periphery of the crystal. This makes it possible to reduce the level of of dark current of n^+- GR due to the reduction of the area of collection of charge carriers from the surface. But a significant decrease in the dark current of REs was not observed in such cases. We proposed to carry out boron diffusion in the gaps between REs and between REs and n^+-GR.

Keywords: silicon, photodiode, dark current, guard ring.

Received 18 May 2023; Accepted 26 October 2023.

Introduction

In recent decades, interest in the development of devices capable of recording light fluxes of low power has grown in the world. This task is effectively performed by silicon photodetectors, widely used representatives of which are *p-i-n* photodiodes (PD). The parameter that determines the minimum possible level of detected optical radiation is the dark current (I_d). This parameter may depend on various factors: the area of the responsive element (RE), the degree of doping of the RE [1], the presence of defects on the surface and volume of the substrate, the presence of uncontrolled impurities introduced during the production of the RE [2], etc.

The reverse (dark) current in *p-n*-junctions is formed due to the thermal generation of pairs of free charge carriers in the space charge region (SCR) [3] and next to the SCR (at a distance of the order of the diffusion length of the charge carriers). This generation occurs through deep energy centers of generation - *recombination, which are located near the middle of the band gap of the semiconductor. The greatest contribution to the formation of the reverse current of *p-n*-junction of REs is made by those areas in which the lifetime of charge carriers is minimal. Usually, the minimum lifetime of charge carriers is on surfaces with a high rate of surface recombination. If the edges of the planar *p-n*-junction of the RE extend to such a surface, then precisely these edge areas can be the site of the predominant generation of the reverse current.

The PD dark current consists of three components: diffusion, volumetric generation-recombination (I_d^G) and surface (surface-generation) (I_d^{surf}). I_d^{surf} can be determined with formula (1) [2]:

$$I_d^{surf} = \frac{eN_{ss}v_{drift}\sigma_{ss}A_{p-n}}{2} \quad (1)$$

where e is electron charge, v is the drift speed of charge carriers, σ_{ss} – capture cross-sectional area, N_{ss} – density of

surface states, A_{p-n} – is the area that contributes to the surface component of the dark current.

As can be seen from (1) I_d^{surf} directly proportional to the density of surface states and the collection area of charge carriers on the surface. But this area can change greatly due to the formation of an *n*-type inversion layer on the surface of high-resistance *p*-Si, which forms surface conductive channels due to the presence of charge in the passivating SiO_2 and at the Si-SiO_2 interface. The formed inversion layer in contact with the n^+-RE increases the area of the responsive element along the surface. With a sufficient amount of positive charge and expansion of the inversion channel over the entire area of the crystal, it is possible to increase the area of the RE along the surface to the edge of the crystal.

The general reasons for the appearance of inversion layers are known and studied [4, 5]. The key factor in their formation is an increase in specific resistance, since with an increase in ρ of the material, a smaller amount of impurities is needed to change the surface conductivity to the opposite [6]. In most cases, an inversion layer is already present on *p*-type silicon with ρ=1-10 Ω·cm [7]. In the case of thermal operations, the technological reasons for the appearance of inversion are improper chemical treatment of substrates, the presence of alkali metal impurities in deionized water, quartz ware, or a quartz reactor, and carrier gases. The probability of the appearance of inversion layers can be minimized by careful control of carrier gases, deionized water for the presence of alkali metals, and periodic purging of quartz reactors with hydrochloric acid vapors.

In addition to the described measures to prevent the appearance and influence of the inversion layer, it is proposed to use the so-called guard rings (GR), which "cut off" the surface channel and limit the surface component of the dark current. Initially, GRs systems were used in power transistors to increase the breakdown voltage [8, 9]. In particular, modeling of a powerful *n*-channel DMOS-transistor with a drain-to-drain breakdown voltage of more than 870 V is presented in [8], while the described transistor had a system with 7 GRs. With the development of solid-state electronics and the growing need for products, in particular, photoreceivers with high operating voltage, guard rings were borrowed into other areas. Thus, in [10], the simulation of the construction of *p*-Si-based avalanche PDs with four n^+-type and one p^+-type GRs for recording low-power light fluxes is given. In [11], a diode with a Schottky barrier with floating guard rings was investigated. A system of 23 GRs is formed, and EBIC analysis shows that the electric field disappears at the 5th GR, making the next 17 rings unimportant.

Guard rings are also borrowed for the technology of silicon *p-i-n* PDs. In particular, in [12] a silicon *p-i-n* PD with two GRs was modeled and investigated, and in [13] an *n*-Si-based *p-i-n* PD with 3 GRs was studied: two - *p*+-type and one peripheral n^+- type. When examining industrial samples, it was seen that some PDs are manufactured without an GR (GD QP154-Q, First, Germany [14]) or with one GR (PD YAG-555-4, Excelitas Technologies Corp, Taiwan [15]). So from the literature and technical sources, it was seen that opinions about the structure of the guard ring system of photodetectors differ greatly, therefore, taking into account the need of the industry for the development and production of high-reliability silicon *p-i-n* PDs, it was decided to experimentally investigate the influence of the guard ring system on the parameters of the PD, in particular, the dark currents of REs.

I. Experimental

The research was carried out in the manufacture of silicon quadrant *p-i-n* PDs for operation at reverse bias U_{bias}=120 V based on *p*-type conductivity silicon with a specific resistance ρ≈16-20 kΩ·cm and and crystallographic orientation [111]. The thickness of the substrate reached 460-480 microns. The technological route of PD manufacturing consisted of a combination of thermal operations and photolithography. Initially, silicon substrates were oxidized according to the principle of dry-wet-dry [16] oxidation to form a masking coating with a thickness of h_{SiO2}≈0.7-0.8 μm. Further, after photolithography, a two-stage diffusion of phosphorus from planar sources in a nitrogen atmosphere was carried out to form REs and an n^+-type GR. The surface concentration of the impurity after the first stage of diffusion (formation of a thin surface highly alloyed layer) was N_0=1.1-1.3·10^{21} cm^{-3}. The next stage of phosphorus diffusion in a dry oxygen atmosphere at a higher temperature to increase the depth of the n^+-*p*-junction, redistribution of the impurity and the formation of anti-reflective coating, the surface concentration of the impurity after this operation was N_0 = 4-4.5·10^{20} cm^{-3} [1]. Further, after chemical dynamic polishing of the reverse side of the substrate, boron diffusion is carried out to create a p^+-type ohmic contact and heterogenization of generation-recombination centers [17]. The next operation is sputtering of Cr-Au with a Cr underlayer to form contacts, then welding the leads to the contact pads, assembly work, placing the crystal in the case and sealing.

For the formation of p^+-GR, boron was additionally diffused into the front side of the substrate.

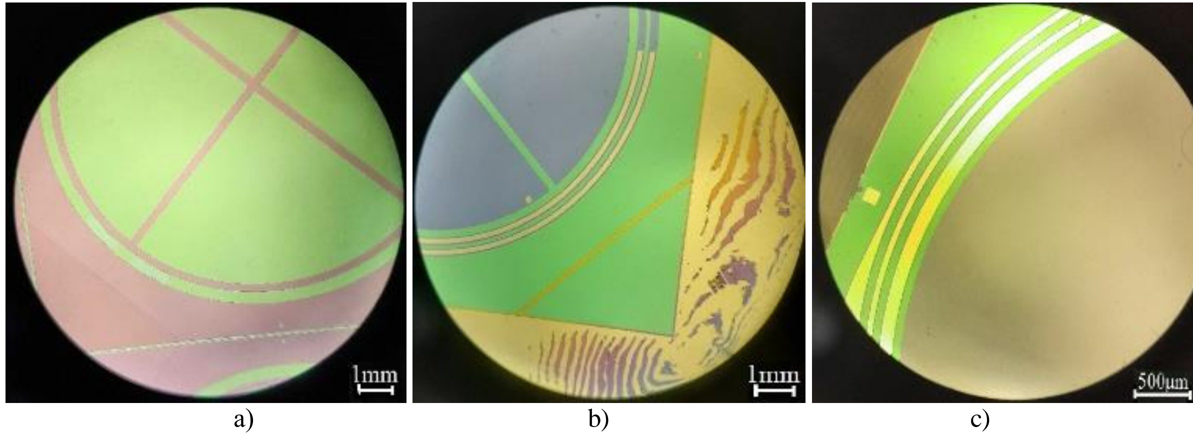
Various combinations of n^+- and p^+- GRs systems were studied.

II. Research results and discussion

2.1. Photodiodes with n^+-guard rings

The level of I_d of the RE depends on the level of the dark current of the GR (I_{GR}), since in the presence of inversion layers, the flow of charge carriers from the GR into the RE is possible. This is especially observed at elevated temperatures due to the increase in the conductivity of inversion channels. To compare the dark current levels of REs and GR from the structure of the guard ring system, a PD with one, two and three n^+-GRs was made (Fig. 1).

In the case of one n^+-GR, charge carriers are "collected" by this element during the reverse bias not only from the area of the GR, but also from the periphery of the crystal (covered with an inversion layer), the ends and half of the gap between the GR and the REs. The collection of charge carriers occurs due to the expansion of the SCR of GR with an increase in U_{bias} both in the



a) b) c)

Fig. 1. Image of a FD crystal with one n^+-GR (a), two n^+-GRs (b), three n^+-GRs (c).

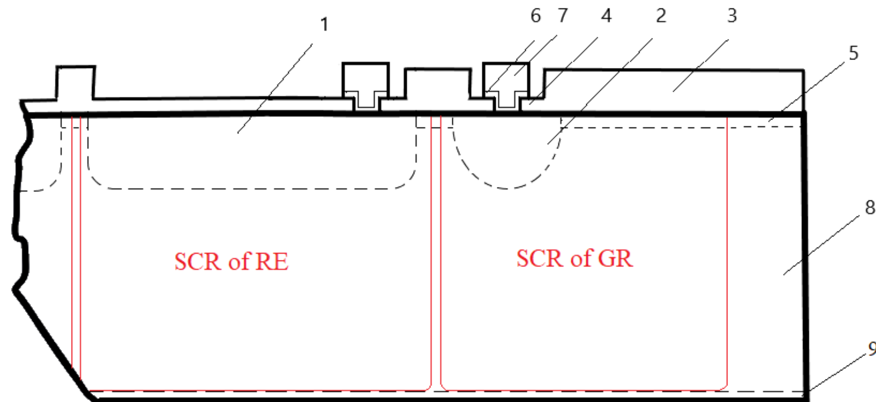


Fig. 2. Schematic section of a part of the PD crystal: 1 – n^+-RE; 2 – n^+-GR; 3 – masking SiO_2; 4 – anti-reflective SiO_2; 5 – n^+-inversion layer; 6 – chrome sublayer; 7 – contact surface-Au; 8 – p-Si substrate; 9 – ohmic p^+-Si.

thickness of the crystal and to the periphery (Fig. 2).

Note that with a low U_{bias} and a large size of the periphery of the crystal, SCR of GR does not reach the edge of the crystal. The width of the SCR (W_i) can be determined from the equation (2) [1]:

$$W_i = \left(\frac{2\varepsilon\varepsilon_0\,(\phi_c - U_{bias})}{eN_A}\right)^{\frac{1}{2}} \qquad (2)$$

where ε, ε_0 is dielectric constants for silicon and vacuum, respectively; φ_c is contact potential difference; N_A is concentration of acceptors in the substrate.

So, in the case shown in Fig. 1(a), the distance from the GR to the edge of the crystal is 800 μm. And for a substrate with specific resistance $\rho \approx 18$ kΩ·cm ($N_A = 7.7 \cdot 10^{11}$ cm^{-3}) and U_{bias}=120 V according to equation (2), $W_i \approx 490$ μm. Note, that after thermal operations, a certain decrease in the specific resistance of the base material [18] is possible, which will slightly reduce W_i. So, in the described case, the charge carriers from the ends of the crystal do not participate in the formation of I_{GR}.

The volt-ampere (IV) characteristics of the dark current of the REs (I_d of each RE are the same) and GR of the photodiode with one n^+-GR (Fig. 3, 4).

From Fig. 3, it can be seen that the IV curve for n^+-GR does not reach saturation. This indicates that with an increase in the reverse bias voltage, W_i will increase, which will contribute to the growth of I_{GR} until the SCR reaches the edge of the crystal. At the moment of expansion of SCR of GR to the entire periphery of the crystal, the IV curve of GR will reach saturation.

In the case of IV characteristics of REs (Fig. 4), the curve reaches saturation at the moment of reaching the SCR of the reverse side of the crystal, accordingly, further growth of the volumetric generation component of the dark current does not occur, which can be seen from equation (3) [2]:

$$I_d^G = e\frac{n_i}{2\tau}W_i A_{RE} \qquad (3)$$

where n_i is intrinsic concentration of charge carriers in the substrate; τ is lifetime of minor charge carriers, A_{RE} is responsive element area.

In the case of the production of PD with two and three n^+-GRs, a decrease in I_d of REs was not observed. But a slightly different picture was observed when measuring the IV characteristics of the GRs (Fig. 5):

The external GR had a level of dark current approximately the same as in the case of a one n^+-GR. And the IV curve of the internal GR was similar to the volt-ampere characteristic of the RE with a slightly lower level of dark current (I_{GR}=15 nA) due to the reduction of the active area. The saturation of the IV curve of the inner GR is also caused by the expansion of the SCR to the opposite side of the crystal and the limitation of the SCR from the side of the outer GR and REs. A similar pattern was observed in the case of three n^+-GRs.

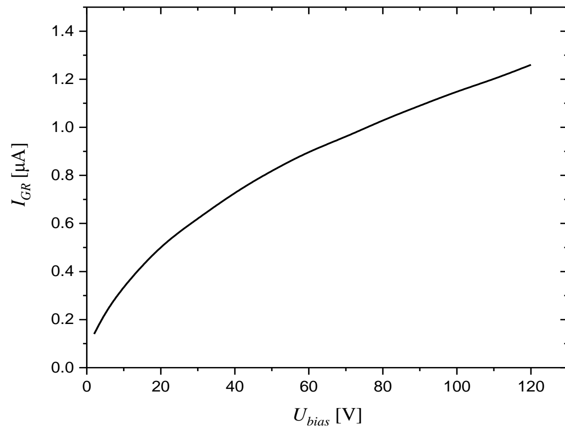


Fig. 3. IV characteristics of n^+-GR.

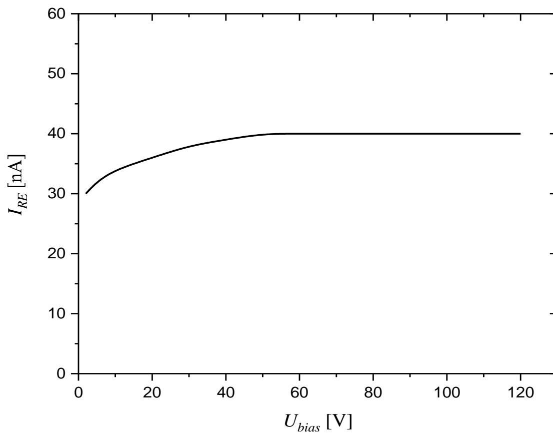


Fig. 4. IV characteristics of REs of PD with one n^+-GR.

Therefore, increasing the amount of n^+-GRs does not affect the dark current of the REs. But we note that with an increase in the number of n^+-GRs, the probability of an edge breakdown of the n^+-p-junction in the regions of the exit of the hetero-junction of the GRs to the surface increases. Since the p-n-junction, due to the presence of an oxide etching wedge, comes to the surface at an acute angle. These areas are places of localization of an increased level of electric field intensity, respectively, areas with reduced breakdown voltage [19]. When several n^+-GRs are formed, the perimeter of the region of the n^+-p-junction exit to the surface increases, so it is worth using a PD crystal structure with one n^+-GRs.

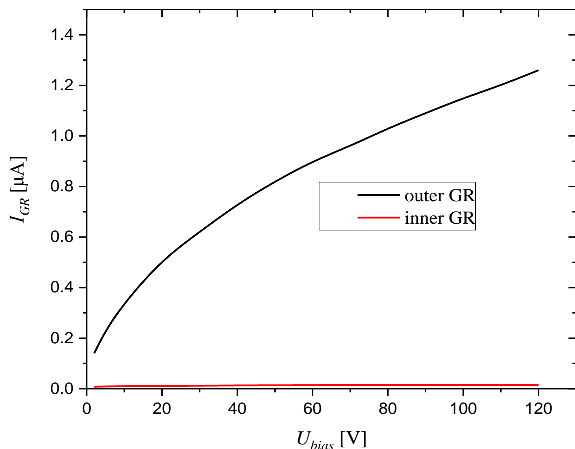


Fig. 5. IV characteristics of GRs of PD with two n^+-GRs.

2.2. Photodiodes with a combination of n^+- and p^+-guard rings.

It is possible to reduce the levels of dark current of REs and GR by combining n^+- and p^+- protective areas. Consider the structure of a PD crystal with two n^+-GRs and one p^+-GR (PD_1). Moreover, p^+-GR is located on the periphery of the crystal (Fig. 6a). This p^+-GR is a region of restriction of the dark current leakage channels, isotypic with the substrate material.

This topology of the PD crystal allows to slightly reduce the level of the dark current of the external n^+-GR due to the reduction of the surface generation component, since the p^+-GR limits the surface area covered by the inversion layer from which the n^+-GR collects charge carriers. As a result of the reduction of I_{GR}, some reduction of I_d of RE (as well as internal I_{GR}) is possible, but this reduction is not significant. Note that p^+-GR should be placed at a distance from n^+-GRs smaller than W_i.

To effectively reduce the dark current of the GR, it is necessary to form a p^+-region on the entire periphery of the crystal (Fig. 6b) (PD_2). The minimum distance from the n^+-region at which the p^+-layer can be formed is the sum of the lateral diffusion of phosphorus and boron under the oxide mask [20]. As the p^+-region approaches the n^+-GR, the area of capture of charge carriers by the guard ring decreases. Also, the diffusion of boron to the front side of the substrate with subsequent thermal operations is a process of gettering, where the p^+-region acts as a getter [17]. This makes it possible to reduce the number of generation-recombination centers in the volume of the periphery of the crystal, and accordingly, the I_d^G of GR.

When producing FD with p^+-layers on the front side of the crystal, we suggested diffusion of boron into the gaps between the REs and between the REs and n^+-GR (Fig. 7) (PD_3). The production of samples with this topology does not introduce additional technological operations, it is only necessary to change the photo template. This makes it possible to increase the insulation resistance of the REs between themselves, and the photocoupling coefficient increases accordingly. The isolation resistance between GR and REs is also increasing. Thus, without the p^+-region, the insulation resistance of all REs and GR with a gap of 200 μm between them reaches 2-15 MΩ. And in the case of the formation of the same gap in the middle of the p^+-region with a width of 100 μm - 18-50 MΩ. Such a crystal structure should be used at increased levels of charge in the oxide, which makes it impossible to influence the inversion channels on the dark currents of the REs and GR.

To study the levels of dark currents of PDs with a combination of n^+- and p^+-guard rings, *IV* characteristics of GR (Fig. 8) and REs (Fig. 9) was obtained. As can be seen from Fig. 8, PD_3 with p^{+-} regions on the periphery of the crystal and in the gaps between active elements have the lowest level of dark current. This is caused by a decrease in the area of capture of charge carriers on the surface by the guard ring and gettering of the generation and recombination centres in the volume of the crystal periphery. But the values of I_{GR} PD_2 and PD_3 differ minimally.

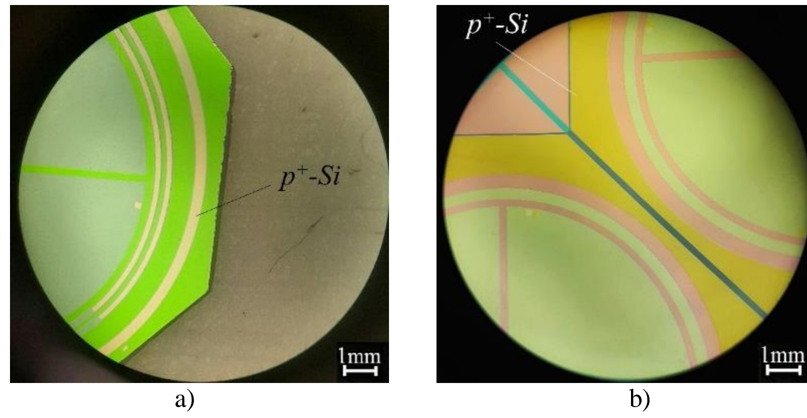
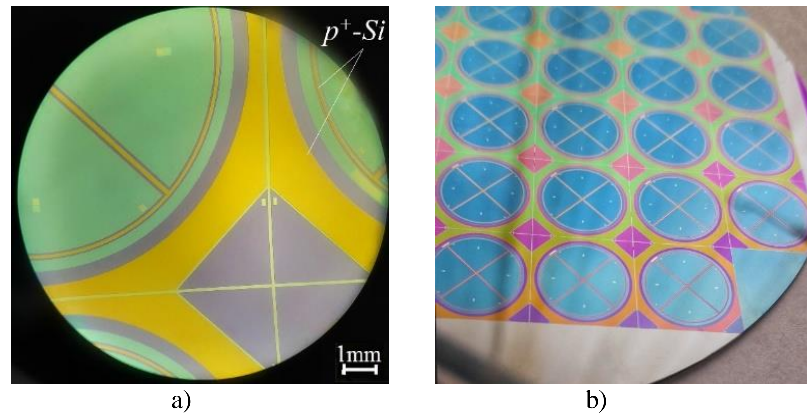


Fig. 6. Image of a PD crystal: with one p^+-GR and two n^+-GRs (a); PD crystal with one n^+-GR and p^+-region on the entire periphery.



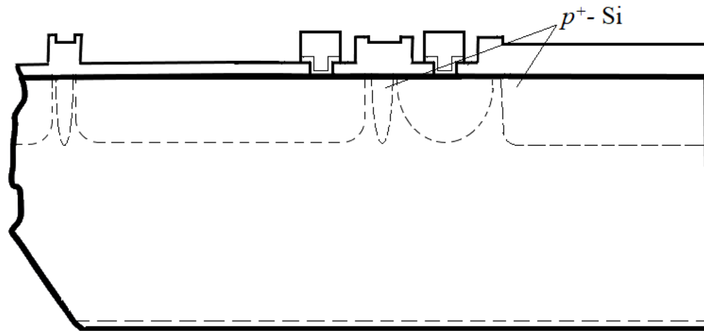


Fig. 7. Image of a PD crystal with p^+-region between active elements and on the periphery:
a) a fragment of a crystal;
b) plate with completed crystals;
c) schematic section.

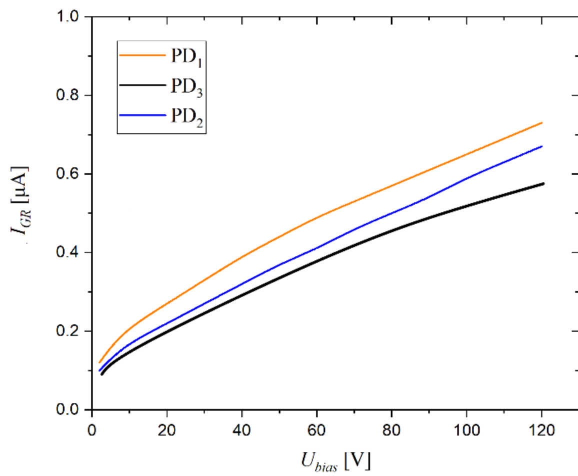


Fig. 8. IV characteristics of GRs of PD with a combination of n^+- and p^+- guard regions.

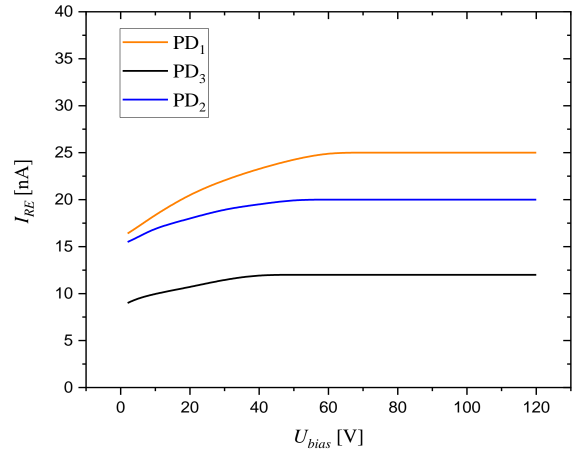


Fig. 9. *IV* characteristics of REs of PD with a combination of n^+- and p^+-guard regions.

A different picture was observed during the study of *IV* characteristics of REs (Fig. 9). I_d of REs of PD_3 were two times lower than in PD_1, and somewhat lower than in PD_3 due to minimization of the influence of inversion channels on dark currents. Accordingly, the structure of the guard ring system with a combination of n^+- and p^+-regions as in PD_3 allows obtaining the lowest dark currents of GR and REs from the considered cases.

Conclusions

The impact of the guard ring system structure on the dark currents of REs and the actual GR of silicon 4-element *p-i-n* PDs was investigated. The following conclusions were made during the investigation:

1. Increasing the number of n^+-GRs does not affect the dark current of REs. The structure with one n^+-GR is optimal.

2. With an increase in the number of n^+-GRs, the probability of an edge breakdown of the n^+-*p*-junction in the regions of the exit of the hetero-junction of the GR to the surface increases.

3. It is possible to reduce the dark current levels of REs and GR by combining n^+- and p^+- protective areas. To effectively reduce the dark current of the GR, it is necessary to form a p^+ -region on the periphery of the crystal.

4. When conducting boron diffusion into the gaps between the REs and between the REs and n^+-GR. it is possible to increase the insulation resistance of the REs between themselves, as well as the insulation resistance between the GR and the REs. Such a crystal structure should be used at increased levels of charge in the oxide, which makes it impossible to influence the inversion channels on the dark currents of the REs and GR. PDs with this topology have the lowest levels of dark currents of REs and GR of the considered cases.

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[1] M.S. Kukurudziak, *Influence of Surface Resistance of Silicon p-i-n Photodiodes n+-Layer on their Electrical Parameters*, Physics and chemistry of solid state, 23(4), 756 (2022); https://doi.org/10.15330/pcss.23.4.756-763.
[2] M.S. Kukurudziak, *Formation of Dislocations During Phosphorus Doping in the Technology of Silicon p-i-n Photodiodes and their Influence on Dark Currents*, Journal of nano- and electronic physics, 14(4), 04015(6cc) (2022); https://doi.org/10.21272/jnep.14(4).04015.
[3] Zi S.: Semiconductor physics. Moscow, *Mir* (1984) [in Russian].
[4] V.M. Lytvynenko, I.M. Vikulin, *Influence of surface properties on reverse characteristics of semiconductor devices*, Bulletin of the Kherson National Technical University, (1), 46 (2018) [in Ukrainian].
[5] Yu.O. Kruglyak, M.V. Strikha, *Physics of nanotransistors: gate voltage, surface potential, and mobile electronic charge in bulk MOS and thin SOI*, Sensor electronics and microsystem technologies, 16(2), 5 (2019); https://doi.org/10.18524/1815-7459.2019.2.171224 5.
[6] M.S. Kukurudziak, *1064 nm wavelength p-i-n photodiode with low influence of periphery on dark currents.* Journal of nano- and electronic physics, 14(1), 01023(4pp), (2022); https://doi.org/10.21272/jnep.14(1).01023.
[7] M.M. Atalla, E. Tannenbaum, E.J. Scheibner, *Stabilization of Silicon Surfaces by Thermally Grown Oxides,* Bell System Tech. J. 38, 749 (1959).
[8] N. L. Lagunovych, *Optimization of the design of guard rings and the specific resistance of the epitaxial film of a powerful n-channel DMOP transistor*, Bulletin of the National Academy of Sciences of Belarus. Series of physical and technical sciences. 65(1), 97 (2020); https://doi.org/10.29235/1561-8358-2020-65-1-97-103 [in Russian].
[9] B.S. Avset, *The effect of metal field plates on multiguard structures with floating p+ guard rings, Nucl.* Instrum. Methods Phys. Res., Sect. A. 377(2–3), 397 (1996); https://doi.org/10.1016/0168- 9002(96)00194-5.
[10] N.N. Korytko, V.B. Zalessky, V.S. Malyshev, V.V. Khatko, *Simulation of the design of avalanche photodiodes with guard regions for recording low-power light fluxes,* Instruments and measurement methods, 1(2), 32 (2011) [in Russian].
[11] Driche, Khaled, et al. *Electric field distribution using floating metal guard rings edge-termination for Schottky diodes*, Diamond and Related Materials, 82, 160 (2018); https://doi.org/10.1016/j.diamond.2018.01.016.
[12] F. Rezaei, Dehghan Nayeri, F., Rezaeian, A. *A novel design of a silicon PIN diode for increasing the breakdown voltage,* IET Circuits, Devices & Systems, 16(6), 491 (2022); https://doi.org/10.1049/cds2.12120.
[13] I.B. Chistokhin, K.B. Fritsler, *Influence of getter formation conditions in high-resistance silicon on the characteristics of PIN photodiodes*, JTP Letters, 46(21), 11 (2020); https://doi.org/10.21883/PJTF.2020.21.50188.18455 [in Russian].
[14] Data Sheet YAG-555-4. Electronic resource. Access mode: https://www.excelitas.com/product/yag-555-4-series-quadrant-photodiodes-si-pin-141-mm.
[15] Data Sheet QP154-Q. Electronic resource. Access mode: https://www.first-sensor.com/en/products/optical-sensors/detectors/quadrant-pin-photodiodes-qp/.
[16] S.W. Glunz, F. Feldmann, *SiO_2 surface passivation layers–a key technology for silicon solar cells*. Solar Energy Materials and Solar Cells, 185, 260 (2018); https://doi.org/10.1016/j.solmat.2018.04.029.

[17] M.S. Kukurudziak, E.V. Maistruk. *Features of Diffusion Doping and Boron Gettering of Silicon p-i-n Photodiodes*, 2022 IEEE 3rd KhPI Week on Advanced Technology (KhPIWeek), 1 (2022); https://doi.org/10.1109/KhPIWeek57572.2022.9916420.
[18] G.P. Gaidar, *Effect of different modes of heat treatment on the Hall parameters and lifetime of charge carriers of transmutationally doped silicon crystals*, Journal of physical research, 22(4), 4601 (2018);. https://doi.org/10.30970/jps.22.4601 [in Ukrainian].
[19] T. M. B.agaev, A. A. Abdreymov, *Modeling microplasmas pn junction*. EPRA International Journal of Multidisciplinary Research (IJMR), 8(6), 139 (2022); http://dx.doi.org/10.36713/epra2013.
[20] V. Jeyaselvan, S.K. Selvaraja, *Lateral Dopant Diffusion Length Measurements Using Silicon Microring Resonators*, IEEE Photonics Technology Letters. 30(24), 2163 (2018); https://doi.org/10.1109/LPT.2018.2879574.

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Вплив структури охоронних кілець на темнові струми кремнієвих *p-i-n* фотодіодів

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У статті досліджено вплив структури системи охоронних кілець (ОК) на темнові струми чутливих елементів (ФЧЕ) та власне охоронних кілець кремнієвих 4-елементних *p-i-n* фотодіодів (ФД). Зразки виготовлені на основі *p*-кремнію за планарною технологією. Виготовлено зразки з одним, двома та трьома ОК. Було встановлено, що збільшення кількості n^+-ОК не зменшує темновий струм ФЧЕ. Але зі збільшенням кількості n^+-ОК збільшується ймовірність крайового пробою n^+-*p*-переходу в областях виходу гетеропереходу ОК на поверхню. Зменшити рівні темнового струму ФЧЕ та ОК можна шляхом поєднання захисних областей n^+- та p^+-, де p^+-ОК є областю обмеження каналів витоку темнового струму, ізотипних з матеріалом підкладки. ФД виконано з p^+-ОК по периферії кристала у вигляді концентричного кільця, а також з p^+-областю по всій периферії кристала. Це дозволяє знизити рівень темнового струму n^+-ОК за рахунок зменшення площі збору носіїв заряду з поверхні. Але істотного зменшення темнового струму ФЧЕ в таких випадках не спостерігалося. Нами запропоновано здійснювати дифузію бору в проміжках між ФЧЕ та між ФЧЕ та n^+-ОК.

Ключові слова: кремній, фотодіод, темновий струм, охоронне кільце.