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Could the negative capacitance effect be used in field-effect transistors with a ferroelectric gate?

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We analyze the electric potential and field, polarization and charge, and differential capacitance of a silicon metal-oxide-ferroelectric field effect transistor (MOSFET), in which a gate insulator consists of thin layers of dielectric SiO_2 and weak ferroelectric HfO_2. It appeared possible to achieve a quasi-steady-state negative capacitance (NC) of the HfO_2 layer, $C_{HfO_2} < 0$, if the layer thickness is close to the critical thickness of the size-induced ferroelectric-paraelectric phase transition. However, this effect disappears as the gate voltage increases above a certain critical value, which can be explained by the nonlinearity of the ferroelectric permittivity. The quasi-steady-state NC corresponds to a positive capacitance of the whole system. Implementation of the gate insulator NC, C_{ins}, can open the principal possibility to reduce the MOSFET subthreshold swing below the critical value, and to decrease the gate voltage below the fundamental Boltzmann limit. However, we failed to found the parameters for which C_{ins} is negative in the quasi-steady states; and thus, the negative C_{HfO_2} cannot reduce the subthreshold swing below the fundamental limit. Nevertheless, the increase in C_{ins}, related with $C_{HfO_2} < 0$, can decrease the swing above the limit, reduce device heating during the operation cycles, and thus contribute to further improvements of MOSFET performances.

Keywords: negative capacitance, ferroelectric film, size-induced phase transition, metal-oxide-ferroelectric field effect transistor.

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Introduction

In recent years, there have been intense attempts to create devices that would use a negative capacitance (**NC**) effect [1, 2, 3, 4] predicted by Rolf Landauer as early as 1976 [4]. If successful, such attempts would lead to a real breakthrough in the scaling of modern electronic devices [5, 6]. In particular, the use of thin ferroelectric films has been proposed for this purpose, since they can maintain ferroelectric properties at the thicknesses of 5 nm or even less; are CMOS-compatible and thermally stable in combination with silicon; allow deposition on 3D substrates; have a wider band gap than silicon and form a significant contact barrier for the electrons from the silicon conduction band. The principal possibility of reduction (in case of success) the subthreshold swing and supply voltage to the values below the fundamental limits define the great interest in the creation of these systems using ferroelectrics [7].

Thin films of a CMOS-compatible "weak" ferroelectric HfO_2, which spontaneous polarization, depending on the conditions, is within the range 2 – 40 μC/cm^2, band gap is equal to 5.8 eV, electron affinity to vacuum ~2 eV, and relative dielectric permittivity is about 25, are very promising candidates for metal-oxide-ferroelectric field effect transistors (MOSFETs) [8, 9, 10, 11]. Below we consider a silicon MOSFET, in which the gate insulator consists of thin layers of a dielectric SiO_2 and a weak ferroelectric HfO_2. We study the possibility of implementing a stable NC of the insulator in such a

system, which would open the principal possibility to reduce the subthreshold swing to the values below the threshold, 60 mV/decade at room temperature, and supply voltage to the values below the fundamental Boltzmann limit, 0.5 V, which would be an important step towards further miniaturization of MOSFETs.

I. Problem formulation

The scheme of the transistor in which the gate insulator is formed from thin layers of a passive dielectric SiO_2, a weak ferroelectric HfO_2, and a p-type silicon semiconducting channel is shown in Fig. 1(a). Figure 1(b) shows the heterostructure for the case of flat bands [12, 13], when the gate voltage of flat bands (FB) is applied. The voltage is determined by the difference between the work-function of the gate and the semiconductor channel, as well as by the surface charge at the HfO_2 – Si interface. We regard that the surface charge is due to the bound charge, created by the polarization P_3 in the ferroelectric layer, which depends on the gate voltage, and neglect the charge on the electron traps at the interface. Thin dielectric SiO_2, ferroelectric HfO_2, and p-type semiconductor silicon layers have the thickness d, h and t, respectively. Their relative dielectric permittivity are ε_e, ε_b ("background") and ε_s, respectively. Electric potentials are denoted as $\phi^{(e)}$, $\phi^{(i)}$ and $\phi^{(s)}$, respectively.

The ferroelectric film is regarded either paraelectric or single-domain, that is a very probable assumption for thin HfO_2 films. For both cases it is characterized by an inhomogeneous one-component spontaneous polarization, $P_3(x,z)$, perpendicular to film surfaces.

The spatial distribution and evolution of the spontaneous polarization is described using Landau-Ginzburg-Devonshire (LGD) approach and electrostatic equations. The system of electrostatic equations governing the potential distribution have the following form:

$$\varepsilon_0\varepsilon_e\left(\frac{\partial^2}{\partial z^2}+\frac{\partial^2}{\partial x^2}\right)\phi^{(e)}=0,\quad -h-d\le z\le -h, \tag{1a}$$

$$\varepsilon_0\varepsilon_b\left(\frac{\partial^2}{\partial z^2}+\frac{\partial^2}{\partial x^2}\right)\phi^{(i)}=\frac{\partial P_3}{\partial z},\quad -h\le z\le 0, \tag{1b}$$

$$\varepsilon_0\varepsilon_s\left(\frac{\partial^2}{\partial z^2}+\frac{\partial^2}{\partial x^2}\right)\phi^{(s)}=-e(Z_dN_d^+-n-Z_aN_a^-+p),\ 0\le z\le t. \tag{1c}$$

The dielectric permittivities are $\varepsilon_e=3.9$, $\varepsilon_b=7$, $\varepsilon_s=11.8$. Concentrations of the immobile ionized donors and acceptors inside the channel are N_d^+ and N_a^-, respectively; the charge densities of mobile free electrons and holes, are n and p, respectively. When the electric current is absent, the charge densities depend on the electric potential $\phi^{(s)}$ in the conventional way [14] (see Appendix A in [15] for details). To model the semiconducting properties of the channel we use the following parameters: acceptor concentration $N_{a0}=10^{24}$ m^{-3}, their ionization degree $Z_a=1$ and energy level $E_a=-1.05\,eV$; donor concentration $N_{d0}\ll 10^{20}$ m^{-3}, band gap $E_g=1.1\,eV$. The bottom of the conduction band is selected as zero energy. The boundary conditions to Eqs.(1) are itemized below.

(a). The potential $\phi^{(e)}$ at the top of is poly-Si gate is equal to the applied potential, V_G, $\phi^{(e)}(-H)=V_G$, where $H\gg h$. The potential $\phi^{(e)}$ at the n$^+$ poly-Si gate – SiO_2 interface, $z=-h-d$, is equal to the potential difference:

$$\phi^{(e)}\big|_{z=-h-d}=V_G-V_{FB}\equiv V_g, \tag{2a}$$

where V_{FB} is equal to the flat-band potential, and we regard that $V_{FB}\approx 1$eV for estimates. Below, for the sake of simplicity we recall V_g as a reduced gate voltage, keeping in mind that it is differs from the potential V_G applied to the top surface of the n$^+$ poly-Si gate. The introduction of V_g in Eq.(2a) allows us to model the three-layer structure, consisting of SiO_2, HfO_2 layers, and p-Si channel, instead of the realistic four-layer structure, shown in Fig. 1(b).

(b) The electric potential is continuous at the HfO_2 - p-Si and SiO_2-HfO_2 interfaces, $z=-h$ and $z=0$, respectively (see e.g. [16]):

$$\left(\phi^{(e)}-\phi^{(i)}\right)\big|_{z=-h}=0 \text{ and } \left(\phi^{(i)}-\phi^{(s)}\right)\big|_{z=0}=0 \tag{2b}$$

The bottom surface of the channel is grounded, $\phi^{(s)}\big|_{z=t}=0$. The electric current in the channel of length L is controlled by the source-drain potential difference, $\phi^{(s)}(x=0)-\phi^{(s)}(x=L)=V_{ds}$.

(c) The electric displacement is also continuous at the insulator interfaces, $z=-h$ and $z=0$:

$$\left(-\varepsilon_0\varepsilon_b\frac{\partial\phi^{(i)}}{\partial z}+P_3+\varepsilon_0\varepsilon_e\frac{\partial\phi^{(e)}}{\partial z}\right)\Big|_{z=-h}=0,$$

$$\left(-\varepsilon_0\varepsilon_b\frac{\partial\phi^{(i)}}{\partial z}+P_3+\varepsilon_0\varepsilon_s\frac{\partial\phi^{(s)}}{\partial z}\right)\Big|_{z=0}=0. \tag{2c}$$

(d) It should be noted that the edges of conduction and valence bands must have jumps related with the differences of corresponding Fermi levels and electron affinities at the HfO_2 - p-Si and SiO_2-HfO_2 interfaces, respectively:

$$\chi_i-\chi_s\approx 1.05\text{ eV},\quad \chi_i-\chi_s\approx -2.05\text{ eV}. \tag{2d}$$

These conditions influence the breaks of carrier

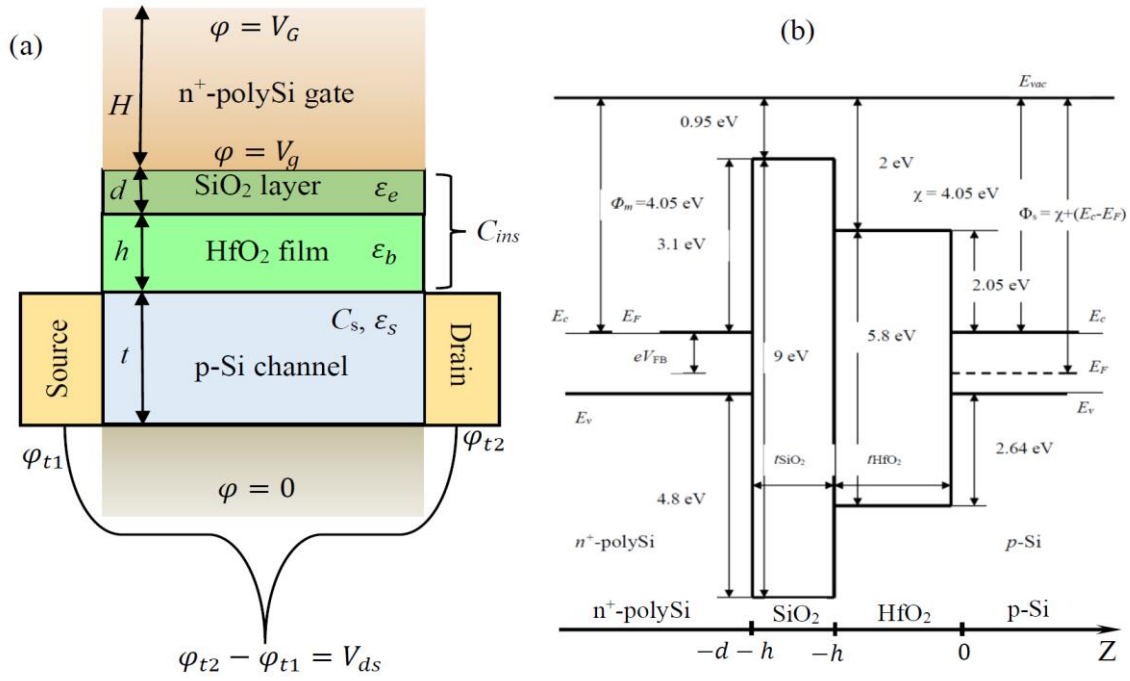

Fig. 1. The geometry and band diagram of the considered FET, consisting of the n^+ poly-Si gate, dielectric SiO_2 layer, ferroelectric HfO_2 film, and the p-type Si channel.

concentrations at the interfaces. In the absence of currents, these conditions follow from the conditions of local electrochemical potential (Fermi quasi-levels) continuity.

The LGD equation governing the polarization distribution has the form:

$$\Gamma\frac{\partial P_3}{\partial \tau} + \alpha P_3 + \beta P_3^3 + \gamma P_3^5 - g\frac{\partial^2 P_3}{\partial z^2} - g^*\frac{\partial^2 P_3}{\partial x^2} = -\frac{\partial \phi^{(i)}}{\partial z}, \quad -h \le z \le 0, \tag{3a}$$

Here Γ is the Khalatnikov kinetic coefficient [17], and the corresponding Landau-Khalatnikov relaxation time τ_K of polarization reversal can be introduced as $\tau_K = \Gamma/|\alpha|$. The coefficient $\alpha = \alpha_T(T - T_C)$. The switching time τ_K can be estimated as $10^{-9} - 10^{-10}$ seconds far from the Curie temperature T_C. However, this estimate works for a single-domain defect-free ferroelectric HfO_2. Due to the different pinning mechanisms the defect-limited switching kinetics is determined by much higher switching times, e.g., microseconds. Thus, below we analyze the quasi-static polarization response, when the period of applied voltage is much higher than τ_K.

LGD coefficients of HfO_2:Si were determined from experimental data, as described in Appendix B in Ref. [15]. They are: $\alpha_T = 1.72 \times 10^6$m/(F K), $T_c = 334$ K, $\beta = 1.013 \times 10^{10}$ C^{-4}·m^{5}J, $\gamma = 0$, and $g = 5{\times}10^{-10}$ m^3/F. We vary thicknesses in the range d =(5 – 10) nm, h =(10 – 100) nm, t=30 nm and regard that T=300 K.

We use the so-called natural conditions for the ferroelectric polarization,

$$\left(\frac{\partial P_3}{\partial z}\right)\Big|_{z=-h,0} = 0, \tag{3b}$$

that support a single-domain state in the HfO_2 film, and neglect the carrier presence inside the dielectric and ferroelectric layers, while considering the top gate electrode as an ideal metal.

Formally, the differential capacitance of the considered heterostructure is given by expression

$$C = \frac{dQ}{dV_g}, \tag{4a}$$

where Q is the charge of the top electrode. This charge, taken with the opposite sign, is equal to the sum of the bottom electrode charge Q_b, and total space charge in the channel Q_s, $Q = -Q_b - Q_s$. Assuming that the serial expression for the capacitance is valid:

$$\frac{1}{C} = \frac{1}{C_{ins}} + \frac{1}{C_s} \tag{4b}$$

where C_{ins} is the differential capacitance of the insulator, consisting of the ferroelectric and dielectric layers, and C_s is the differential capacitance of the channel. The serial expression for the capacitance, $1/C_{ins} = 1/C_{SiO_2} + 1/C_{HfO_2}$, is not rigorous if domains are present due to the non-local permittivity of the ferroelectric layer, which characterizes the whole system, but not its separate parts [18]. However, we can use the expression as the upper estimate of the ferroelectric layer differential capacitance, C_{HfO_2}, and put $C_{SiO_2} = \frac{\varepsilon_0\varepsilon_e}{d}$ for the dielectric layer. The channel

capacitance is $C_s \cong \frac{dQ_s}{d\varphi_s}$, where φ_s is the potential drop, and Q_s is the total space charge of the channel. Roughly, the channel capacitance can be estimated as $C_s \approx \frac{\varepsilon_0 \varepsilon_s}{w}$, where w is the voltage-dependent thickness of the space-charge screening layer.

From the above estimates, the differential capacitances C_{ins} and C_{HfO_2} are

$$\frac{1}{C_{ins}} = \frac{1}{C} - \frac{1}{C_s}, \quad C_{ins} = \frac{C}{1-\frac{C}{C_s}}, \tag{4c}$$

$$\frac{1}{C_{HfO_2}} \approx \frac{1}{C_{ins}} - \frac{1}{C_{SiO_2}} = \frac{1}{C} - \frac{1}{C_s} - \frac{1}{C_{SiO_2}}, \quad C_{HfO_2} \approx \frac{C}{1-\frac{C}{C_s}-\frac{C}{C_{SiO_2}}}. \tag{4d}$$

The effect of the negative ferroelectric capacitance means that $C_{HfO_2} < 0$, meanwhile the total capacitance C must be positive in the thermodynamic equilibrium, because the stable NC of the system part can be achieved only consistently with positive electrostatic energy and capacity of the entire system [19]. For the same reasons C_{ins} must be positive in a steady-state regime of a two-layer capacitor structure (see e.g., Ref. [20] and refs therein), while any thermodynamic limitations on its sign is absent in the considered three-layer structure, and so the situation $C_{ins} < 0$ is not excluded.

II. Results of the finite-element modelling for zero source-drain voltage

Typical results of the self-consistent finite-element modelling (FEM) of the electric potential, ferroelectric polarization, and space charge density in the considered system under the absence of source-drain voltage, $V_{sd} = 0$, are shown in Figs. 2-3. The figures are calculated for an ultra-thin SiO_2 layer with thickness $d = (1-2)$ nm, room temperature, T=300 K, variable film thicknesses $h = (5-50)$ nm and channel width $t = (10-30)$ nm [21].

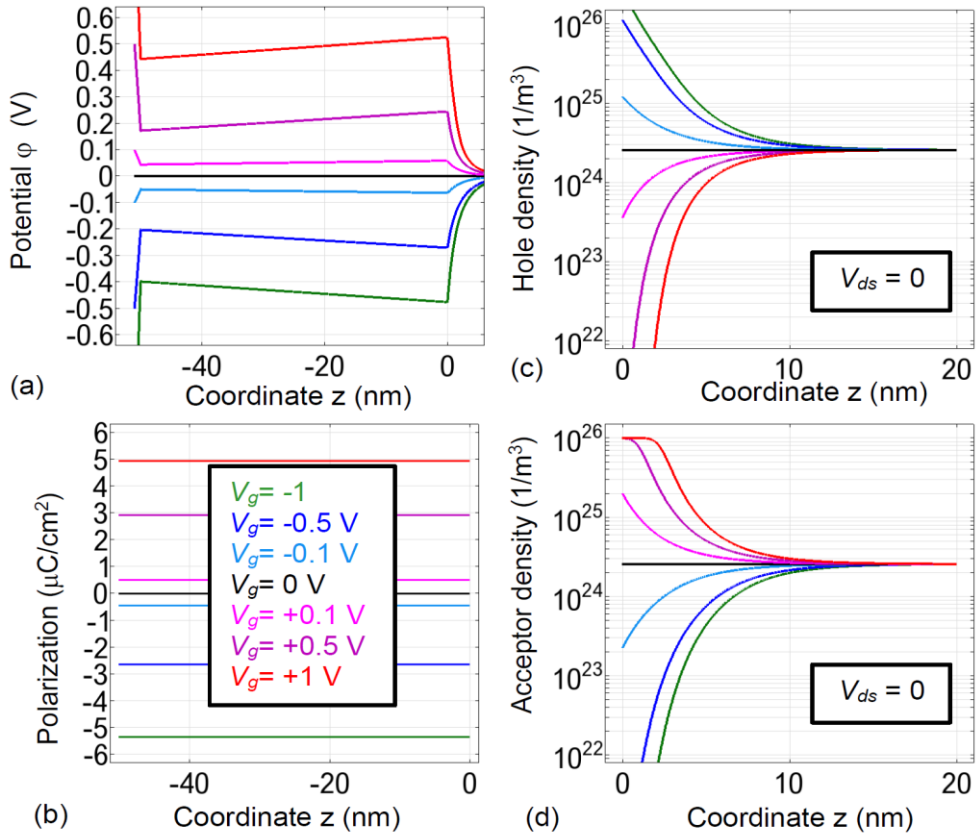

Fig. 2. The effect of electric potential inversion at the dielectric/ferroelectric interface. The distribution of an electric potential in the SiO_2-HfO_2-p-Si heterostructure (a), electric polarization in the HfO_2 layer (b), holes density (c), and ionized acceptors concentration (d) in the p-Si channel calculated for $V_{ds} = 0$ and different reduced gate voltages: V_g = -1 V (dark-green curves), -0.5 V (dark-blue curves), -0.1 V (light-blue curves), 0 (black curves), +0.1 V (magenta curves) and +1 V (red curves). The HfO_2 thickness h=50 nm and the p-Si thickness t=30 nm.

The electric potential "inversion" at the dielectric/ferroelectric interface is seen in Fig. 2(a), where the sign of the voltage drop in the ferroelectric film is opposite to the signs of the potential drop in the dielectric layer and in the semiconductor channel. That say, potential drops inside the dielectric and ferroelectric layers have different signs, and the local potential is inverted in some cases. Note that the inversion effect is absent at the ferroelectric-channel interface.

Exactly the inversion effect in a ferroelectric layer is treated by many authors as a manifestation of the NC effect [22, 23, 24]. At that the local electric field, as a z-derivative of the potential, is directed against the average field in the HfO_2, while the direction of the field in the dielectric and semiconductor coincides with the direction of the average field. When the ferroelectric film is thin enough ($h \leq 50$ nm), and the dielectric layer is enough thick ($d \geq 1$ nm), the paraelectric phase is either stable or metastable, and so the spontaneous polarization is virtually absent in the static case [see the black curve, $P_3 = 0$, at $V_g = 0$ in Fig. 2(b)]. The field-induced polarization, shown by colored curves in Fig. 2(**b**), is proportional to the local electric field in the HfO_2 film. Under the favorable conditions, the field-induced polarization contributes to the NC effect due to the negative local susceptibility. Free carriers in the channel screen the polarization bound charge and electric field; corresponding distribution of holes density is shown in Fig. 2(c). For the band structure parameters, shown in Fig. 1(b), the calculated electron density appeared negligibly small in comparison with the hole density in the channel. For the same reasons one can neglect the concentration of ionized donors in comparison with the concentration of ionized acceptors, shown in Fig. 2(d).

The NC effect is observed in a ferroelectric layer at moderate gate voltages, $|V_g| \leq 1$ V, as shown in Fig. 2(a). The NC disappears with increasing the gate voltage above 1.5 V. The disappearance can be explained by the influence of the ferroelectric and/or semiconductor nonlinearity, because the susceptibility of the ferroelectric layer decreases with the electric field increase; and the electric field penetration into the channel (i.e., the effective thickness w of the depletion layer) depends nonlinearly on the potential difference.

The distribution of an electric potential in the SiO_2-HfO_2-p-Si heterostructure (a), electric polarization in the HfO_2 layer (b), holes density (c) and ionized acceptors concentration (d) in the p-Si channel calculated for $V_{ds} = 0$ and different reduced gate voltages: V_g = -1 V (dark green curves), -0.5 V (deep blue curves), -0.1 V (blue curves), 0 (black curves), +0.1 V (magenta curves) and +1 V (red curves). The HfO_2 thickness h=50 nm and the p-Si thickness t=30 nm.

Quasi-static dependences of the HfO_2 film polarization, P_3, on the gate voltage V_g is shown in Fig. 3(a). The dependences are calculated either for different film thicknesses h. Polarization curves demonstrate a paraelectric-like dependence on V_g for HfO_2 films with $h \leq 25$ nm independently on the channel widths. The height and slope of very thin ferroelectric hysteresis loops, which appear for thicker films with $h > 25$ nm (e.g., for $h = 50$ nm), depends on the channel width t in a complex way. Note that the thickness for $h = 50$ nm is very close to the critical thickness of the size-induced ferroelectric-paraelectric phase transition. The loops are asymmetric with respect to the gate voltage, and this asymmetry is related with the asymmetry of the electric boundary conditions, because the top surface of HfO_2 film contacts with the dielectric SiO_2 layer, and the bottom surface contacts with the semiconductor p-Si.

Quasi-static dependences of the total differential capacitance, C, on the reduced gate voltage V_g is shown in Fig. 3(b). The capacitance curves rarely demonstrate a paraelectric-like dependence on V_g for considered range of channel widths (one asymmetric maxima located near $V_g = 0$). More often, the curves are ferroelectric-like with two asymmetric maximums. The asymmetry is related with the asymmetry of the polarization curves. The height and separation of these maximums become more pronounced for thicker films with $h > 25$ nm and depend

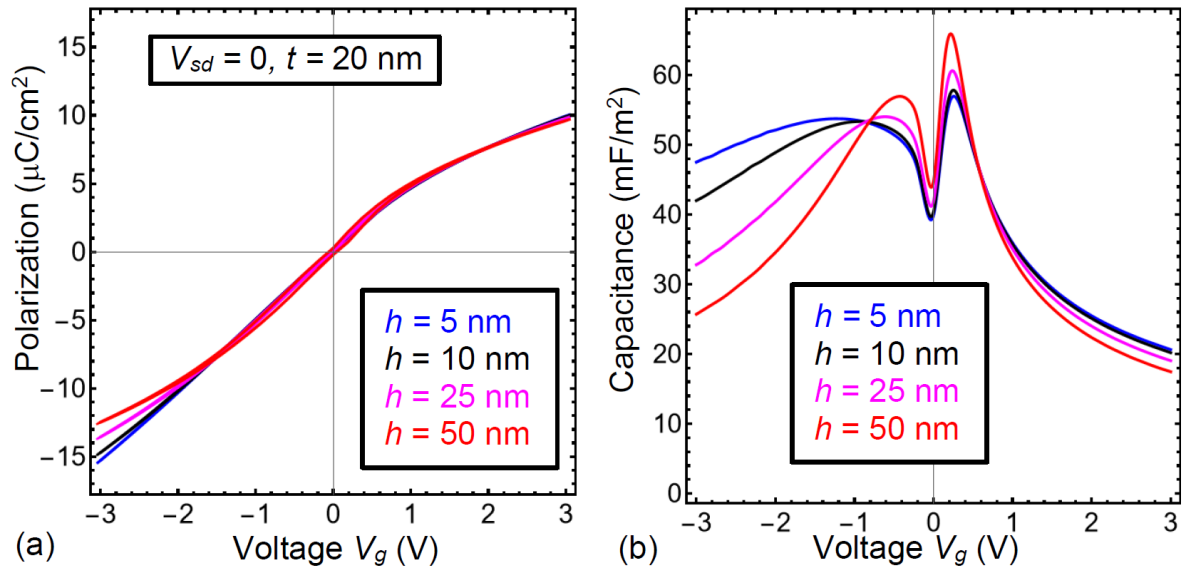

Fig.3. Quasi-static dependences of the HfO_2 film polarization (a) and total differential capacitance (b) vs. the reduced gate voltage V_g calculated for different thickness of HfO_2 film h=5, 10, 25 and 50 nm (blue, black, magenta and red curves, respectively). The channel width t=20 nm.

on the channel width t in a complex way. The total capacitance is positive, and depends on V_g due to the paraelectric or/and ferroelectric nonlinearity in the HfO_2 layer. The capacitance is maximal in the vicinity of $V_g = 0$, because the dielectric susceptibility of the HfO_2 layer is maximal in the voltage range, and decreases significantly with the voltage increase.

III. The influence of the ferroelectric capacitance the MOSFET performances

The source-drain current I_{ds}, as a function of the gate and source-drain voltages, V_g and V_{ds}, can be approximately described by a phenomenological analytical expression:

$$I_{ds} \approx \frac{V_{ds}}{R\left(1+\frac{V_{ds}}{V_s}\right)} F\left(\frac{e(V_g - V_{th})}{k_B T}\right), \qquad (5)$$

where the effective resistance R and the saturation voltage V_s are fitting parameters, and the function F is given by expression:

$$F(\xi) = \frac{(1+\xi^2)}{(1+\xi^2)\exp(-\xi)+1} \approx \begin{cases} \exp(\xi), & \xi \ll -1, \\ \xi^2, & \xi \gg 1. \end{cases} \qquad (6a)$$

The threshold voltage can be estimated as:

$$V_{th} \cong V_{FB} - \phi_{inv}^{(s)} - \frac{P_s\left(\phi_{inv}^{(s)}\right)}{C_{ins}}. \qquad (6b)$$

where C_{ins} is the total capacitance of the ferroelectric and dielectric layers, introduced in Eq.(4b); $\phi_{inv}^{(s)}$ is a potential at the semiconductor surface, $z = 0$, corresponding the inversion of conductivity type in the channel (see e.g., [12]). The NC of a ferroelectric layer, $C_{HfO_2} < 0$, can be reached in the considered heterostructure, because the curves with inverted slope exist inside the ferroelectric layer [see Fig. 2(a)]. In dependence on C_{HfO_2} sign, the inverse capacitances, $\frac{1}{C_{HfO_2}}$ and $\frac{1}{C_{SiO_2}}$, either sum or extract in order to form the inverse total capacitance, $\frac{1}{C_{ins}}$.

Several cases, $C_{HfO_2} < 0$, are shown by blue curves in Fig. 4(a, c) and 4(b, d) for HfO_2 film of thickness h=5 nm and h=50 nm, respectively. A possible physical origin of the observed NC is the situation when the quasi-static charge at the heterostructure top and bottom electrodes increases more slowly than the ferroelectric polarization. Nevertheless $C_{HfO_2} < 0$, the capacitance C_{ins}, calculated for the voltage-dependent differential

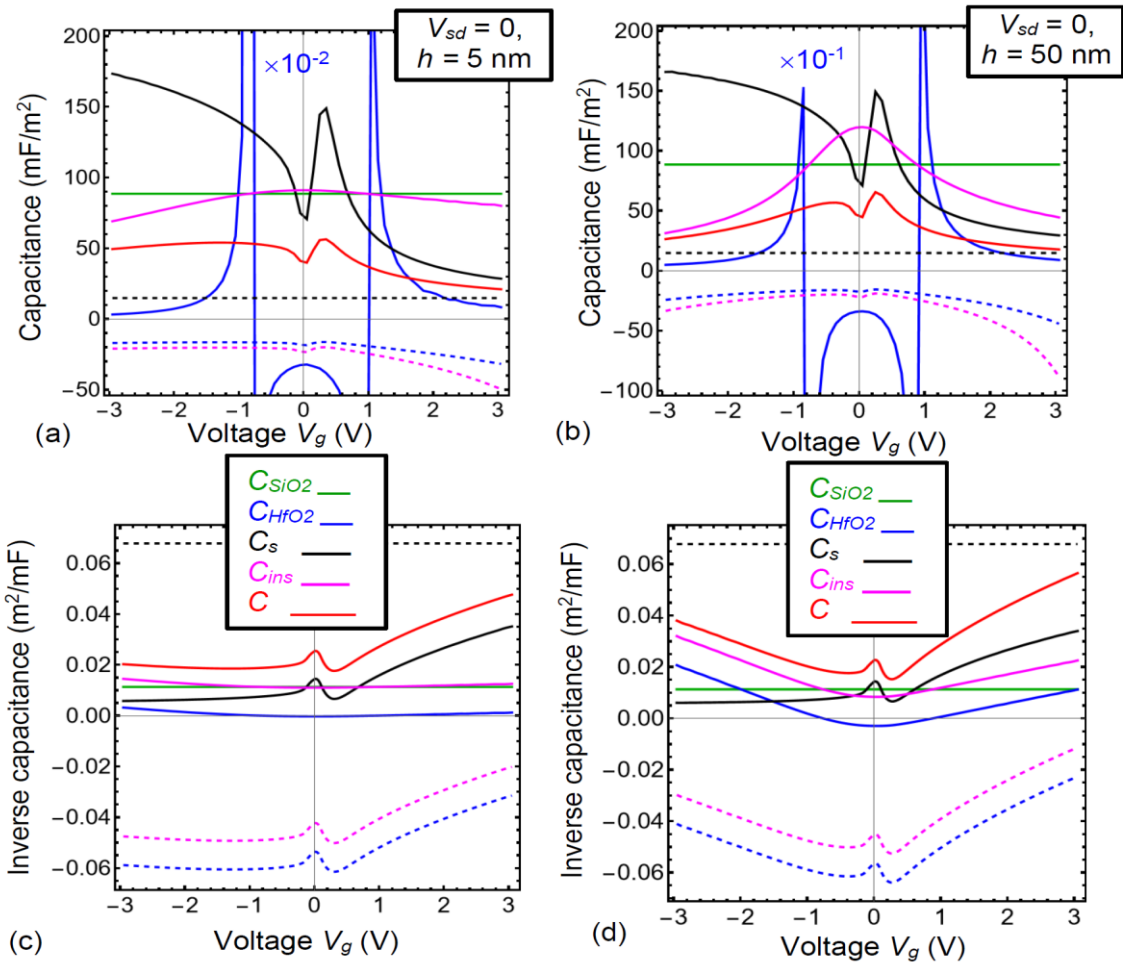

Fig. 4. Quasi-static gate voltage dependence of the direct (a, b) and inverse **(c,** d) differential capacitances C, C_{ins}, C_s, C_{HfO_2} and C_{SiO_2} (solid red, magenta, black, blue and green curves, respectively) on the reduced gate voltage V_g. The HfO_2 film thickness h=5 nm in the plot (a, c) and h=50 nm in the plots (b, d), the channel width t=20 nm. Dashed black, blue and magenta curves are calculated for the constant width of the space-charge layer, $w \cong 12$ nm.

capacitance of the channel, $C_s \cong \frac{dQ_S}{d\varphi_S}$, is positive (see solid black, blue and magenta curves in Fig. 4). The NC, $C_{ins} < 0$, was calculated for the voltage-independent channel capacitance $C_s \approx \frac{\varepsilon_0 \varepsilon_S}{w}$, when the space-charge layer has a constant width $w \cong 12$ nm (see dashed black, blue and magenta curves in Fig. 4). This example shows that the approximation of the space-charge layer with a constant width can lead to a critical mistake in the evaluation of the channel and insulator capacitances.

Next, we estimate the subthreshold swing, S, which characterizes the gate voltage increase to achieve a tenfold increase in the drain current, as [3]:

$$S = \left[\frac{\partial(log_{10} I_{ds})}{\partial V_g}\right]^{-1} = 2{,}3\frac{k_B T}{e}\left(1 + \frac{C_s}{C_{ins}}\right). \qquad (7)$$

For positive C_{ins} the minimum value of S, achieved at $C_s << C_{ins}$, is 60 mV/decade at room temperature. A possible transition to the NC of the insulator part of the heterostructure, $C_{ins} < 0$, would reduce the S value below this limit, which means that the current flow in the “ON” mode will correspond to a lower source-drain voltage V_{ds}. This would reduce the voltage below the fundamental Boltzmann limit of 0.5 V, which would open the possibility of further miniaturization of the MOSFET, currently operating at threshold voltages not less than 0.7 V.

The capacitance C_{ins} must be positive in a steady-state regime, while any thermodynamic limitations on the capacitance C_{ins} of transient states are absent. However, we failed to found the conditions for which $C_{ins} < 0$ either in the steady-state or in the quasi-steady-state (see e.g., the solid magenta curves in Fig. 4). Instead, we obtained the increase of C_{ins} and the decrease of C_s under the simultaneous validity of the conditions $C_{HfO_2} < 0$ and $C_{SiO_2} > 0$ in the vicinity of $V_g \approx 0$ [see the wide maximum at the violet curves and the sharp minima at the black solid curves at $V_g \approx 0$ in Fig. 4]. Since C_{ins} is maximal and C_s is minimal in the vicinity of $V_g \approx 0$, the ratio $\frac{C_s}{C_{ins}}$ is minimal in the vicinity of $V_g \approx 0$, and the condition $0 < \frac{C_s}{C_{ins}} \ll 1$, which decreases S, can be valid at small V_g.

Since the capacitance C_{ins}, but not the NC of the ferroelectric layer itself, determines the FET working performances, and, in particular, the subthreshold swing S, the steady-state NC of a ferroelectric layer cannot reduce S below the fundamental limit. Nevertheless, the increase of C_{ins} can decrease S above the fundamental limit in the case $\frac{C_s}{C_{ins}} \ll 1$; also, it can significantly reduce the transient losses and MOSFETs heating during the operation cycles.

Conclusions

We analyze the distributions of electric potential and field, polarization and charge, and the differential capacitance of a silicon MOSFET, in which a gate insulator consists of thin layers of a dielectric SiO_2 and a weak ferroelectric HfO_2. It appeared possible to achieve a quasi-steady-state NC of a ferroelectric layer if its thick-ness is close to the critical thickness of the size-induced ferroelectric-paraelectric phase transition. The quasi-steady-state NC of the ferroelectric, that is very slow-varying transient state, corresponds to a positive capacitance of the whole system, and so it does not break any thermodynamic principle. Moreover, we have shown that the ferroelectric capacitance becomes positive as the gate voltage increases above a certain critical value, which can be explained by the nonlinearity of the permittivity of ferroelectrics, as well as by the decrease of semiconductor capacitance with the increase of the voltage absolute value.

Since the capacitance of the gate insulator, C_{ins}, but not the NC of the ferroelectric layer itself, determines the FET working performances, implementation of the quasi-steady-state NC C_{ins} can open the principal possibility to reduce the subthreshold swing S below the critical value, and to decrease the gate voltage below the fundamental Boltzmann limit. However, our general conclusion is that $C_{ins} > 0$ in the quasi-steady states, meaning that the NC does not penetrate "outside" the ferroelectric layer of MOSFET, and so it cannot reduce subthreshold swing below the fundamental limit, 60 mV/dec at room temperature. This conclusion agrees with Ref.[19], where it was obtained in the framework of general thermodynamic principles.

Instead, we obtained the increase of C_{ins} under the simultaneous validity of the conditions $C_{HfO_2} < 0$ and $C_{SiO_2} > 0$ at small gate voltages. The increase of C_{ins} can decrease S above the fundamental limit; also, it can significantly reduce the transient losses and MOSFETs heating during the operation cycles.

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Authors' contribution.

A.N.M. and M.V.S. generated the research idea, and A.N.M. formulated the problem mathematically. E.A.E. and L.P.Y. performed FEM. A.N.M. and M.V.S. wrote the manuscript. All co-authors discussed the results.

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Чи можна використовувати ефект негативної ємності у польових транзисторах із сегнетоелектричним затвором?

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Проаналізовано розподіл електричного потенціалу та поля, поляризації та заряду, а також диференціальну ємність кремнієвого метал-оксидно-сегнетоелектричного польового транзистора (MOSFET), в якому підзатворний ізолятор складається з тонких шарів діелектрика SiO_2 та «слабкого» сегнетоелектрика HfO_2. Виявилося можливим досягти квазістаціонарної негативної ємності шару HfO_2, $C_{HfO_2} < 0$, за умови, якщо товщина цього шару близька до критичної товщини фазового переходу сегнетоелектрик-параелектрик, індукованого розміром. Однак також з'ясувалося, що цей ефект зникає, коли напруга на затворі підвищується вище певного критичного значення, що можна пояснити нелінійністю сегнетоелектричної проникності. Квазістаціонарна негативна ємність, яка є дуже повільним перехідним станом сегнетоелектрика, відповідає позитивній ємності всієї системи, і тому її поява не порушує жодного термодинамічного принципу. Реалізація квазістаціонарної негативної ємності C_{ins} ізолятора (діелектрика SiO_2 та «слабкого» сегнетоелектрика HfO_2) може відкрити принципову можливість зменшити підпорогове коливання MOSFET нижче критичного значення та зменшити напругу затвора нижче фундаментальної межі Больцмана. Однак нам не вдалося знайти параметри, для яких ємність C_{ins} є негативною у квазістаціонарних станах; і, таким чином, негативна ємність C_{HfO_2} не може зменшити підпорогове коливання нижче фундаментальної межі. Тим не менш, збільшення C_{ins}, пов'язане з $C_{HfO_2} < 0$, може зменшити коливання вище межі, зменшити нагрівання пристрою під час робочих циклів і, таким чином, сприяти подальшому покращенню продуктивності MOSFET

Ключові слова: від'ємна ємність, сегнетоелектрична плівка, розмірний фазовий перехід, польовий транзистор метал-оксид-сегнетоелектрик.